# BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

**II SEMESTER, 2021-2022**

**Course Handout (Part -11)**

**Date:** 01-01-2022

In addition to Part I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No. : MEL G641

Course Title : CAD for IC Design

Instructor-in-charge : Sumit K Cahtterjee

**Course Description:** Introduction to VLSI design methodologies and supporting CAD tool environment; overview of `C', data structure, graphics and CIF; concepts, structures and algorithms of some of the following CAD tools; schematic editors; layout editors; module generators; silicon compilers; placement and routing tools; behavioural, functional, logic and circuit simulators; aids for test generation and testing.

# Scope and Objective of the course:

To teach the basic concepts of CAD tools used for IC/VLSI Design process. To be conversant with the use of existing CAD tools and algorithms for all the stages of the design cycle of a VLSI chip design, To study modeling using HDL (VHDL/Verilog) and to study the design issues involved in the development of CAD tools., Current trends in CAD tools for IC/VLSI design.

1. **Text Book:**

(i) Algorithm for VLSI Physical Automation, 3rd Edition Author: Naveed Sherwani

Publisher, Year: Kluwer Academic Press, 1998

1. **Reference Books**

(i) An Introduction to CAD for VLSI Author: Stephen M. Trimberger

Publisher, Year: Kluwer Academic Press 1987.

(ii) VLSI Physical Design Automation: Theory and practice Author: Sadiq M Sait and Habib Youssef

Publisher, Year: World Scientific Press, 1999

(iii) Computer Aids for VLSI Design Author: Steven M. Rubin

Publisher, Year: Addison Wesley, 1987

(iv) Simulation in the Design of Digital systems Author: John B. Gosling

Publisher, Year: Cambridge University Press (CUP), 1993

(v) Introduction to VLSI Systems Author: Carver Mead and Lynn Conway Publisher, Year: Addison-Wesley,1980

(vi) A VHDL Primer, 3rd Edition, Author: J. Bhaskar

Publisher, Year: Pearson /Prentice-Hall, 1999

(vii) Verilog HDL Author: Samir Palnitkar

Publisher, Year: Pearson Education Asia, 2007

(viii) Synthesis and Optimization of Digital Circuits Author: Giovanni De Micheli

Publisher, Year: Tata McGraw-Hill, 1994

# Course Plan

|  |  |
| --- | --- |
| **Topics** | **Lectures** |
| An introduction to electronic system design and CAD for IC Design | 1 |
| CAD: A general overview | 1 |
| Partitioning | 4 |
| Floor-planning and Placement | 8 |
| Routing | 5 |
| Schematic, Layout and Stick Editors | 5 |
| Overview of CIF | 1 |
| Simulation  (Behavioral , Functional, Logic, Mixed mode, and Fault simulation) | 4 |
| High Level and logic Synthesis | 4 |
| Hardware Allocation and Assignment | 3 |
| Scheduling and Algorithms | 2 |
| Timing and Power Analysis | 3 |
| TOTAL | 41 |

1. **Evaluation schedule:**

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| --- | --- | --- | --- | --- | --- |
| **EC No.** | **Components** | **Duration** | **Weightage**  **(%)** | **Date & Time** | **Remarks** |
| 1. | Midsem Test | 90 min. | 25% | As per Timetable | Closed Book |
| 2. | Comprehensive Examination | 2 Hrs | 35% | As per timetable | Closed Book |
| 3. | Project/Seminar/Lab Assignments/Quiz | Regular | 40% |  | Open Book |

# Chamber consultation hour: Will be announced in the class.

# Notices: All notices related to the course will be put on the CMS.

1. **Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

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Instructor In-Charge

(MEL G641)